

REMARKS

Reconsideration of the application is respectfully requested.

Claims 1-16 are pending and remain in this application. No claims have been amended, cancelled. Claims 15 and 16 have been added.

Drawings

The Office Action requests corrected drawings. Applicant is submitting herewith corrected formal drawings (Figures 1-12).

Rejections Under 35 U.S.C. § 103

The Office Action has rejected claims 1-14 under 35 U.S.C. § 103(a) as being unpatentable over Beausoleil et al. U.S. Patent 5,551,013 (hereinafter “Beausoleil”) in view of DeHon et al. U.S. Patent 5,742,180 (hereinafter “DeHon”). Applicant respectfully traverses this rejection.

The Office Action has erroneously rejected claims 1 and 9. Neither Beausoleil nor DeHon teach or suggest anything remotely similar to “wave logic for producing a plurality of sequential wave signals, each wave signal corresponding to a row of cells and controlling the propagation of logic signals through the cells of the row”, which is required by claims 1 and 9. The Office Action does not even argue that DeHon discloses such a feature. Indeed, the term “wave logic” is not used anywhere in the Office Action. The Office Action does argue that DeHon discloses “sequential signals corresponding to a row of cells and controlling propagation of logic signals through the cells of that row”. However, other than mimicking the claim language, the Office Action does not state specifically where DeHon discloses such a feature. In

the list of citations provided in the Office Action, Applicant assumes that the descriptions concerning “crossbar (specifically, *CBIN*)” (Figure 4A) and “context identifier (*CID*)” (Figure 5A-5C) in DeHon are what the Office Action asserts corresponds to the above “sequential signals corresponding to a row of cells and controlling propagation of logic signals through the cells of that row”. Regarding crossbar, DeHon describes “the incoming unidirectional *crossbar CBIN* selectively provides eight of the sixteen signals from that adjoining subarray as the eight global signals received by the illustrated subarray” (Col. 10 Lines 25-28) (emphasis added). Regarding *CID*, DeHon describes “Locally, each logic element performs one of a number of locally-stored logic operations as dictated by the *CID*” (Col. 3 Lines 22,23)(emphasis added). Thus, DeHon does not teach either (a) the existence of “*wave logic*”, (b) where the wave logic produces a plurality of “*sequential*” wave signals, or (c) controlling the propagation of logic signals “*through the cells of the row*” as stated in claims 1 and 9. Thus, even if Beausoleil and DeHon are properly combinable, the combination does not teach all elements of claims 1 and 9. Consequently, Applicant respectfully submits the subject matter of claims 1 and 9 would not have been obvious at the time the invention was made to a person having ordinary skill in the art regardless of whether or not there is motivation to combine them.

In addition to the fact that claims 2 and 10 are allowable because the claims they depend from (claims 1 and 9, respectively) are allowable, Applicant adds the following. The Office Action states that DeHon discloses a multiplexer. However, the interconnection logic of claims 2 and 10 is a “*time-multiplexed array*”. DeHon does not teach that the multiplexer disclosed therein is “*time-multiplexed*” as required by claim 2. Indeed, the multiplexers disclosed in DeHon select a specific signal of a plurality of signals (multiplexers L1M1-L1M4, LEM, and OS in Figures 2A and 2B, Col. 6 Lines 37-39, Col 7 Line 56 to Col 8 Line 6). Thus, one having

ordinary skill in the art would recognize that the multiplexers disclosed in DeHon are used to increase the richness of the interconnect and are not used for any time-multiplexing function. Applicant also notes that the multiplexers in DeHon are not arranged in an “array” as required by claims 2 and 10.

In addition to the fact that claims 3, 4, 11 and 12 are allowable because they depend from claims 1 and 9 respectively, which are allowable, Applicant adds the following. The Office Action states that DeHon discloses delay logic and refers the delay flip-flop (DFF) shown in figures 2A and 2B and discussed at Col. 7 Lines 32, 46, 67 in DeHon. DeHon specifically describes the delay flip-flop DFF in Col. 7 Line 27 to Col. 8 Line 3. As is seen in this description, DeHon does not teach or suggest delay logic “for delaying the generation of an Nth sequential wave signal if ... not yet been transmitted” (claims 3 and 11), or “for delaying the generation of an Nth sequential wave signal if ... not yet been received” (claims 4 and 12). Thus, DeHon does not teach the features found in claims 3, 4, 11 and 12.

In addition to the fact that claim 5-8, 13 and 14 are allowable because they depend either directly or indirectly from claim 1 (claims 5-8) or claim 9 (claims 13 and 14), which are allowable, Applicant adds the following. The Office Action states that DeHon discloses time multiplexing in Col. 4 Lines 11-15. However, as discussed above regarding claims 2 and 10, the multiplexers described in DeHon are not time-multiplexed, but instead are used to increase the richness of the interconnect. Furthermore, the Office Action states that DeHon discloses strobe signals in Figure 5C, Col. 5 Lines 61-64. However, figure 5C and the cited passage describe the distribution of an on-chip generated *context* signal. The context signal is generated by a subarray and distributed through combinational and selection logic (Col. 5 Lines 63, 64). In contrast, a strobe line as in claim 6, 8 is a line “for indicating when data is available on a data line”. Thus,

the "context signal" in DeHon is not the same thing as the "strobe line" found in claims 6, 8 and 14.

Based on the foregoing, Applicant respectfully submits that this application is in condition for allowance, which is respectfully requested.


Should the Examiner have any questions or comments on the application, the Examiner should feel free to contact the undersigned via telephone.

Respectfully submitted,

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